## ABSTRACT

One embodiment of the invention is a recursive partitioning method that places circuit elements in an IC layout. This method initially defines a number of partitioning lines that divide an IC region into several sub-regions (also called slots). For a net in the region, the method then identifies the set of sub-regions (*i.e.*, the set of slots) that contain the circuit elements (*e.g.*, the pins or circuit modules) of that net. The set of sub-regions for the net represents the net's configuration with respect to the defined partitioning lines. Next, the placement method identifies attribute or attributes of a connection graph that models the net's configuration with respect to the partitioning lines. The connection graph for each net provides a topology of interconnect lines that connect the slots that contain the net's circuit elements. According to some embodiments of the invention, the connection graph for each net can have edges that are completely or partially diagonal.

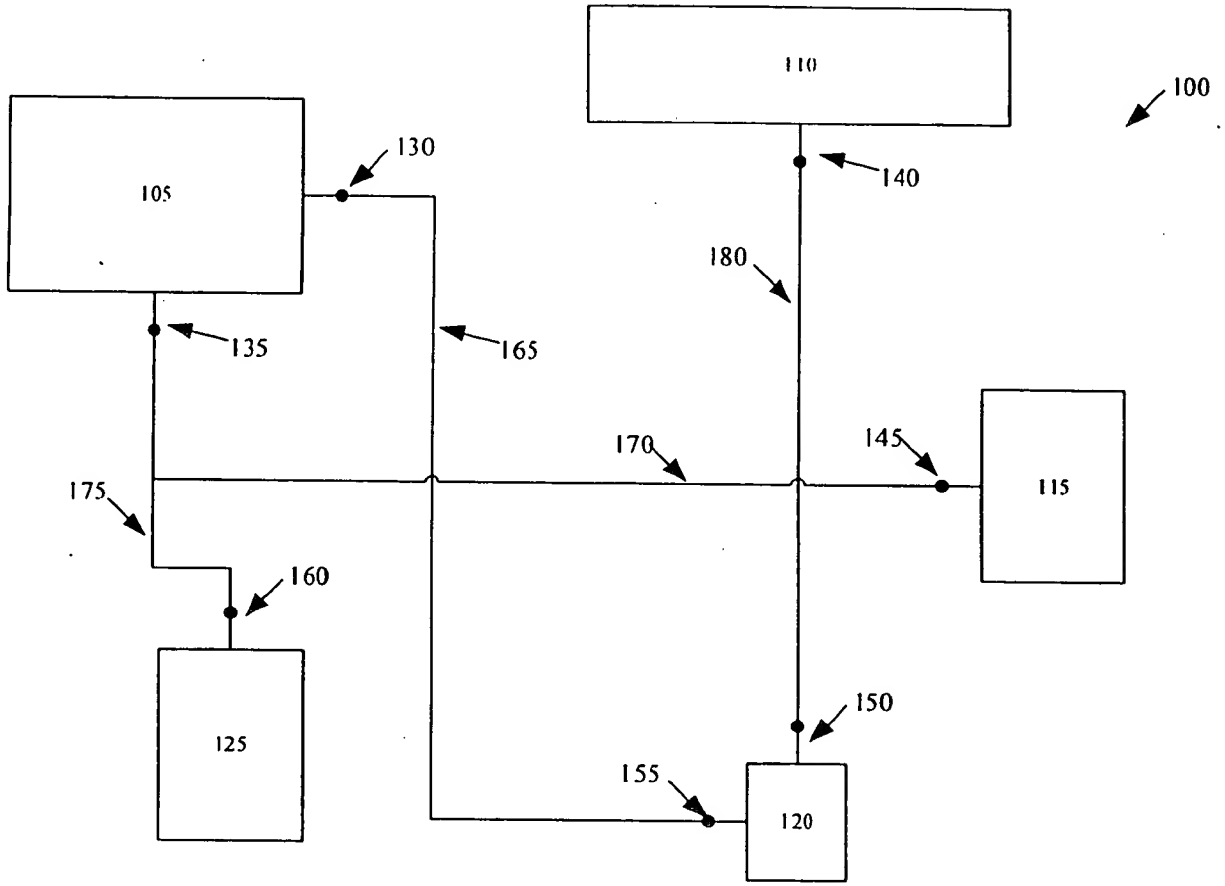
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*Figure 1*